**B-5.**

**RS / D Flip-flop**

**OBJECTIVES:**

The logic circuits that have been used until now were combinational logic circuits since the output of the device depended on the input data. The sequential logic circuit uses positive feedback and thus the output of the device depends on both the input and the previous state of the output. These devices are important since they have two stable states. In this experiment, the student will design, build, and test various sequential logic circuits.

**READING:**

**MATERIALS NEEDED:**

74 LS 00 1 EA

74 LS 02 1 EA

74 LS 04 1 EA

74 LS 08 1 EA

74 LS 76 1 EA

LED 2 EA

330Ω 1 EA

POWER SUPPLY

FUNCTION GERNERATOR

**SUMMARY OF THEORY:**

The flip−flop, also known as a bistable multivibrator, varies from the other digital logic circuits that have been examined since the flip−flop has two stable states or memory. Since these devices have the ability to remember their current state, they are the basic building blocks for registers and Static RAM memory.

***SR latch***



Figure 1 RS flip-flop



Figure 2 RS flip-flop with enabler



Figure 3 Flip-flop with clock

One of the most fundamental latches is the SR latch, where S and R stand for *Set* and *Reset*. Figure 4 shows the logic diagram of an SR latch using cross-coupled NOR gates. The stored bit is available at the output marked Q; its complement is available at output . While the S and R inputs are both low, feedback maintains the two outputs in a constant state.

When R = 1 and S = 0, output Q will go to 0 regardless of its value before R was set to 1, and that forces to 1 after a brief delay. Thus, R resets the output to 0. When R = 0 and S = 1, becomes 0 and Q becomes 1. Thus, input S sets the latch.

When R = S = 1, both Q and become 0, and are no longer complementary to each other. At this point, if both R and S are simultaneously switched to 0, both outputs will be forced to become 1, which in turn will try to force both outputs to become 0, and so on. If both NOR gates and the associated wires have the same delays, both outputs will oscillate indefinitely with a period of 2 gate delays. In reality, the two path delays will not be identical, forcing the latch to go to a stable state. Because the final output state will vary from one latch to another, the input combination R = S = 1 is not usually applied. It is up to the circuit designer to insure that this condition never appears.

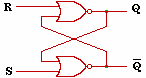
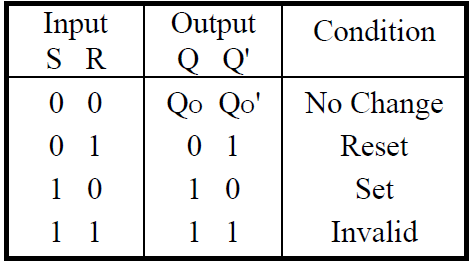
 

Figure 4 SR latch

An alternate model of the SR latch can be built with NAND gates, as shown in Figure 5. *Set* and *reset* now become active low signals, denoted S and R respectively. Otherwise, operation is identical to that of the SR latch. Historically, the NAND-basedlatch has been predominant, despite the notational inconvenience of active low inputs.

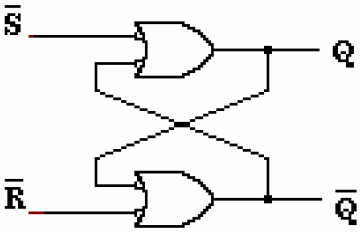
 

Figure 5

The gated SR latch is a latch with an enable input. It behaves the same way as the transparent SR latch provided the enable is asserted. When the enable input is negated, the device is in a hold (the last) state. The logic symbol for the gated SR latch is shown in Figure 2, and the logic diagram and truth table are shown in Figure 6.

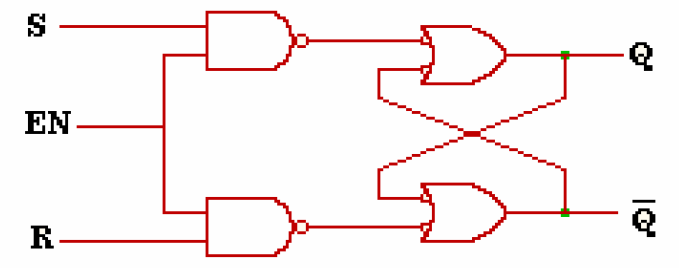
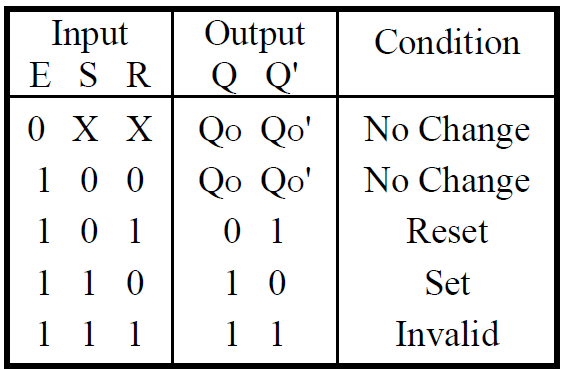
 

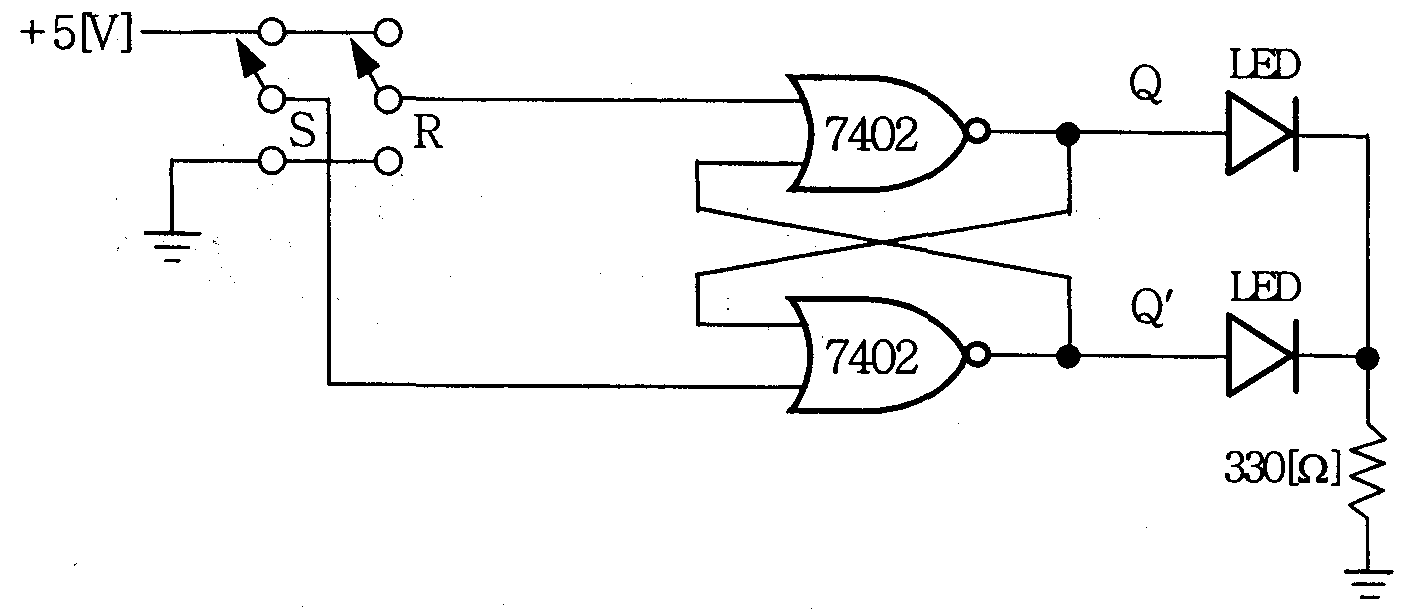
Figure 6

***D-latch***

A D−Latch may be constructed by connecting the R input to the S input through an inverter. There are only two possible states on the output, Set or Reset and there are no disallowed input combinations. By adding a 2−input NAND gate to both inputs of the active low SR latch, we will have an active high, gated SR latch. Figure 6 contains the logic diagram of the active high gated SR latch. This latch will allow the outputs to change states according to the inputs only when the gate is enabled.

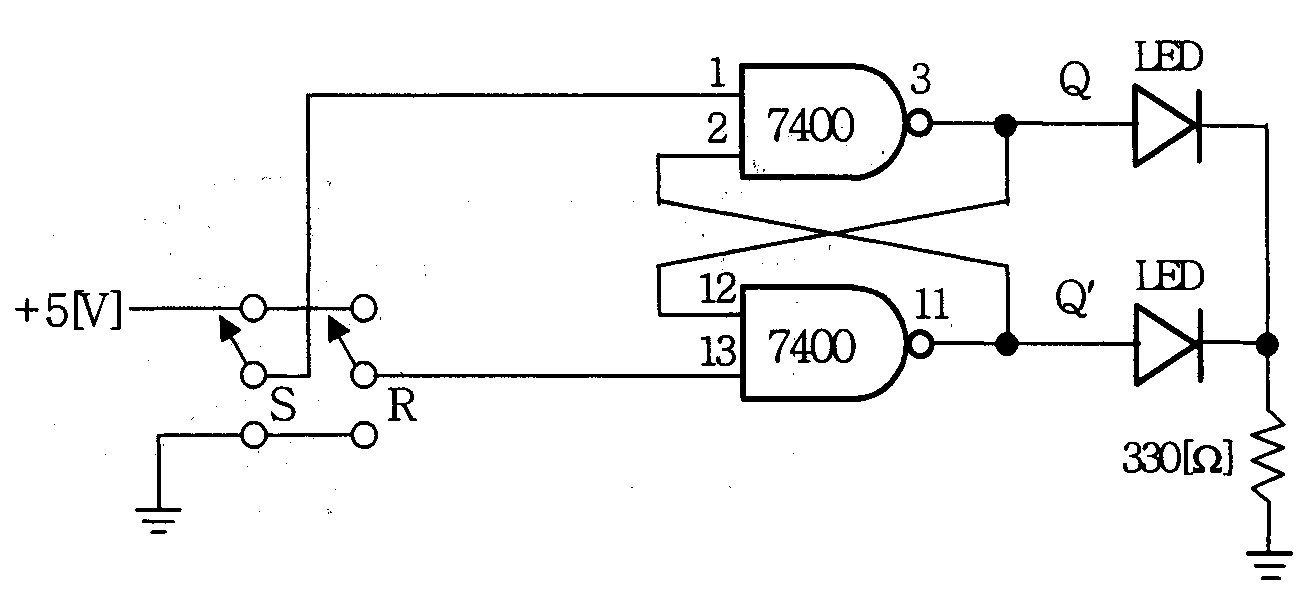
**PROCEDURE**

1. Build RS flip-flop using NOR gates as below figure, and measure the output of the circuit with input R, S and fill the below table out.



|  |  |  |  |
| --- | --- | --- | --- |
| **Input** | | **Output** | |
| **S** | **R** | **Q** |  |
| **1** | **0** |  |  |
| **0** | **0** |  |  |
| **0** | **1** |  |  |
| **0** | **0** |  |  |
| **1** | **1** |  |  |

1. Build RS flip-flop using NAND gates as below figure, and measure the output of the circuit with input R, S and fill the below table out.



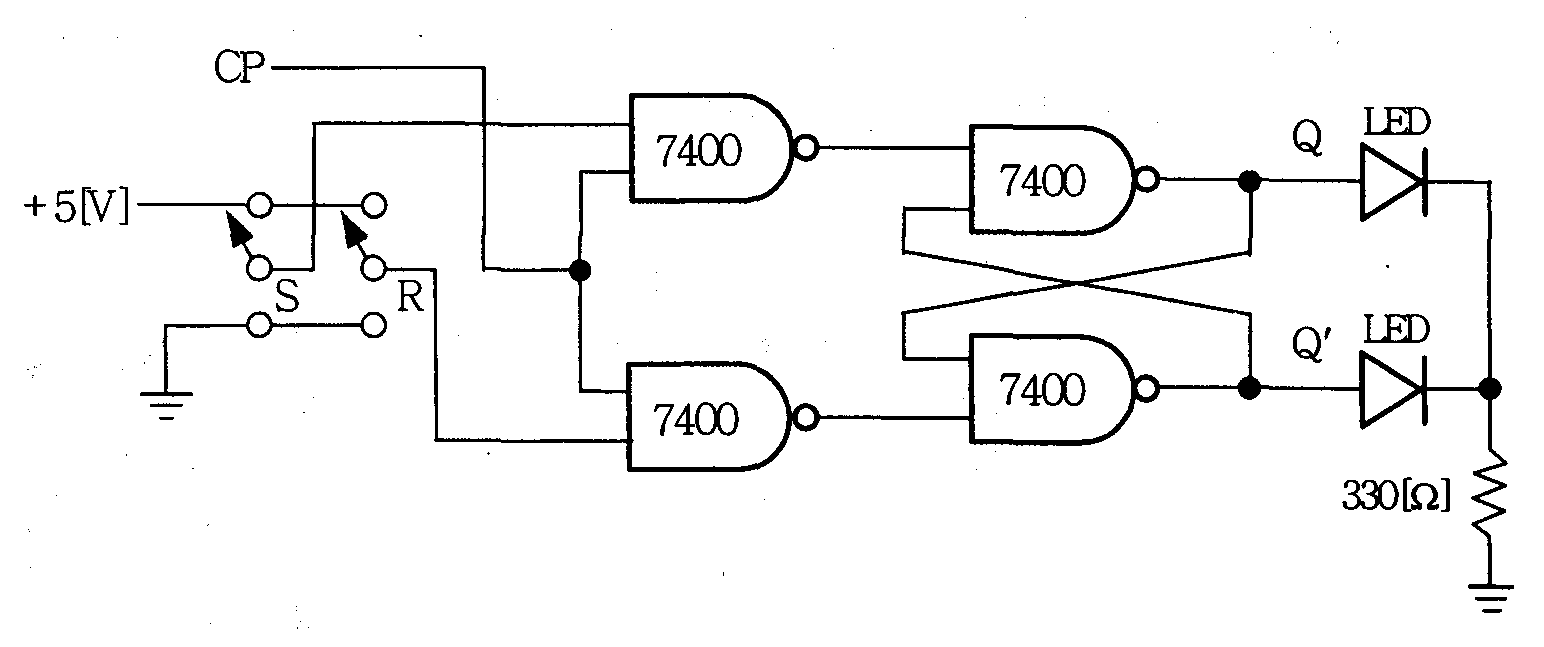
|  |  |  |  |
| --- | --- | --- | --- |
| **Input** | | **Output** | |
| **S** | **R** | **Q** |  |
| **1** | **0** |  |  |
| **0** | **0** |  |  |
| **0** | **1** |  |  |
| **0** | **0** |  |  |
| **1** | **1** |  |  |

1. Build RS flip-flop using NOR gates as below figure, and measure the output of the circuit with input R, S and fill the below table out. Note that an EN input needs to be inserted after S and R voltage are supplied and experiments need to be done sequentially.



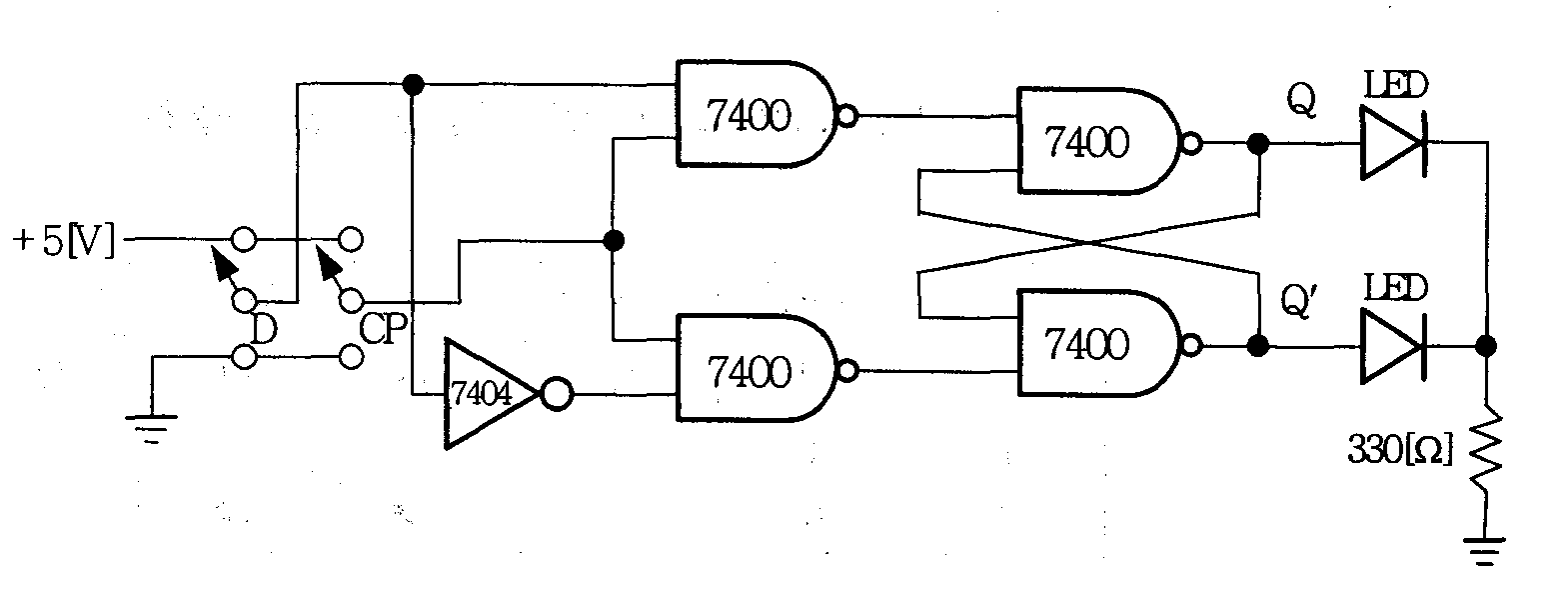
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **EN** | **Input** | | **Output** | |
| **S** | **R** | **Q** |  |
| **0** | **0** | **1** |  |  |
| **0** | **0** |  |  |
| **1** | **0** |  |  |
| **0** | **0** |  |  |
| **1** | **1** |  |  |
| **1** | **0** | **1** |  |  |
| **0** | **0** |  |  |
| **1** | **0** |  |  |
| **0** | **0** |  |  |
| **1** | **1** |  |  |

1. Build RS flip-flop using NAND gates as below figure, and measure the output of the circuit with input R, S and fill the below table out. Note that an CP(Clock Pulse) input needs to be inserted after S and R voltage are supplied and experiment needs to be done sequentially.



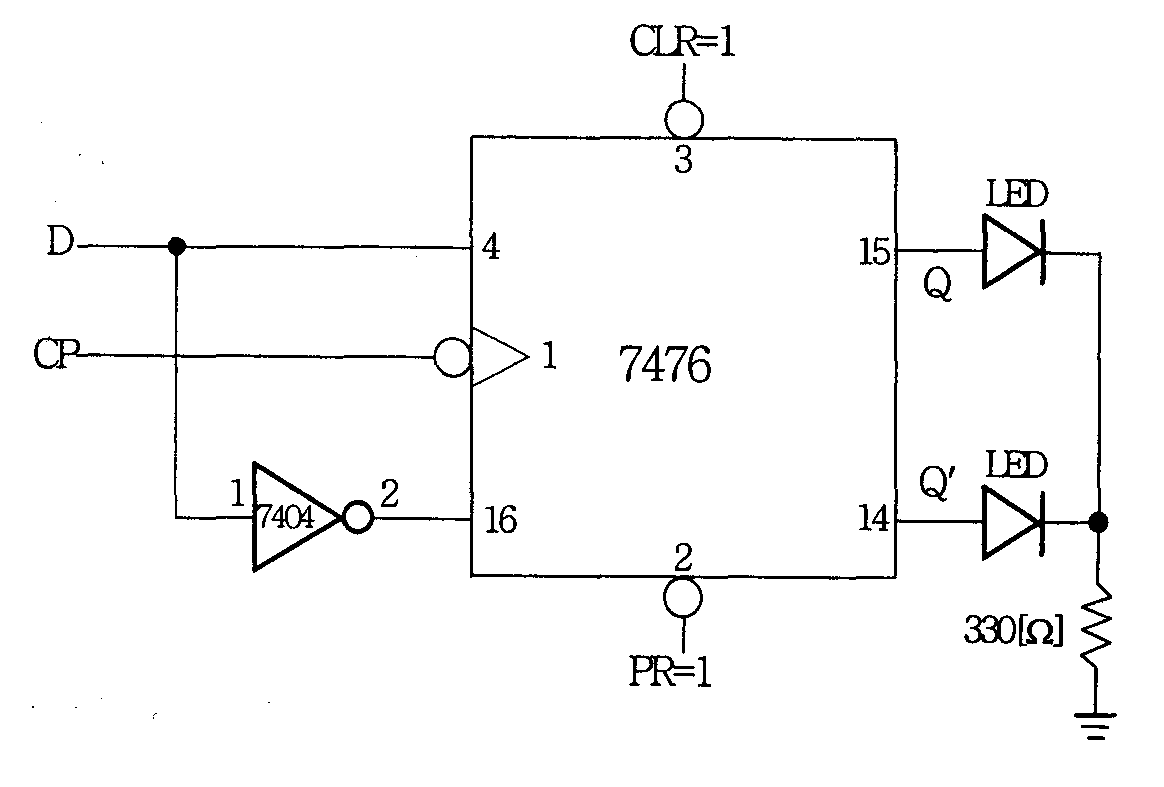
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **CP** | **Input** | | **Output** | |
| **S** | **R** | **Q** |  |
| **0** | **0** | **0** |  |  |
| **1** | **0** | **0** |  |  |
| **0** | **0** | **1** |  |  |
| **1** | **0** | **1** |  |  |
| **0** | **1** | **0** |  |  |
| **1** | **1** | **0** |  |  |
| **0** | **1** | **1** |  |  |
| **1** | **1** | **1** |  |  |

1. Build D flip-flop using NAND gates as below figure, and measure the output of the circuit with input D and CP and fill the below table out.



|  |  |  |  |
| --- | --- | --- | --- |
| **CP** | **Input** | **Output** | |
| **D** | **Q** |  |
| **0** | **0** |  |  |
| **1** |  |  |
| **1** | **0** |  |  |
| **1** |  |  |

1. Build D flip-flop using 7476 as below figure, and measure the output of the circuit with input D and CP and fill the below table out. Note that pin 2(PR), 3(CLR) should be connected to Vcc(+5V)



|  |  |  |  |
| --- | --- | --- | --- |
| **CP** | **Input** | **Output** | |
| **D** | **Q** |  |
| **0** | **0** |  |  |
| **1** | **0** |  |  |
| **1** | **0** |  |  |
| **1** | **1** |  |  |
| **1** | **1** |  |  |
| **0** | **1** |  |  |